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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,199	03/16/2004	Ka Leung Ling	US000192A	3761

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,199	LING ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

preliminary Amend filed

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the abstract exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 21 – 42 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 - 18 of U.S. Patent No. 6,715,001, claims 1 - 20 of U.S. Patent No. 6,732,255, claims 1 - 20 of U.S. Patent No. 6,493,287, and claims 1 - 31 of U.S. Patent No. 6,647,440. Although the conflicting claims are not identical, they are not patentably distinct from each other because as in U.S. Patent No. 6,732,255 contains all the limitations of the current application and continues to further narrow the applications claims by citing CAN microcontroller environment therefore broadening would dictate obviousness.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 35 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 35 recites the limitation "CAN microcontroller" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 38 recites the limitation "CAN/CAL module" in line 18. There is insufficient antecedent basis for this limitation in the claim.

It seems applicant intended to remove the CAN/CAL environment from the claims, however the Examiner will interpret both environments for the purpose of the Office Action.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 21 – 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Baji (US Patent Number 5,513,374).

8. As per claims 21, 41 and 42 a microcontroller, station and system that supports a plurality of message objects, comprising: a processor core that runs applications (multiple processors DSP 1100 and host 1200, figure 1); a module that processes incoming messages (DMAC 3500 processes instructions over buses, figure 1); data memory including a first memory segment that provides a plurality of message buffers associated with respective ones of the message objects (data 1900 and instruction 1400 memory, figure 1), and a second memory segment that provides a plurality of

memory-mapped registers for each of the message objects (instruction memory 1400, figure 1), the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object (memory mapped column 5, lines 54 – 64); and, a memory interface unit (Parallel Arbiter 2100, figure 1) that permits the processor core and the module to concurrently access a different respective one of the first and second memory segments (column 5, lines 7 – 23), and that arbitrates access to the same one of the first and second memory segments when the processor core and the module request concurrent access to the same one of the first and second memory segments (concurrent access and conflicts thereof, column 6, lines 4 – 32, solution through arbitration rules, column 7, lines 1 – 34).

9. As per claims 28, 35, 37, 38 and 40 (interpreted without the CAN/CAL environment) a microcontroller and method that supports a plurality of message objects, comprising: a processor core that runs applications (multiple processors DSP 1100 and host 1200, figure 1); a module that processes incoming messages (DMAC 3500 processes instructions over buses, figure 1), wherein the processor core and the module are contained on a single integrated circuit chip (figure 1); data memory including a first memory space that is located on the integrated circuit chip (data 1900 and instruction 1400 memory, figure 1) and a second memory space that is located off the integrated circuit chip (external memory 2500, figure 1), the first memory space including a first memory segment that provides at least a portion of a message buffer

memory space that includes a plurality of message buffers associated with respective ones of the message objects (instruction memory 1400, figure 1), and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object (memory mapped column 5, lines 54 – 64); and, a memory interface unit (Parallel Arbiter 2100, figure 1) that permits the processor core and the module to concurrently access a different respective one of the first and second memory spaces, that permits the processor core and the module to concurrently access a different respective one of the first and second memory segments (column 5, lines 7 – 23), and that arbitrates access to the second memory space and that arbitrates access to the same one of the first and second memory segments when the processor core and the module request concurrent access to the second memory space or to the same one of the first and second memory segments (concurrent access and conflicts thereof, column 6, lines 4 – 32, solution through arbitration rules, column 7, lines 1 – 34).

10. As per claims 22 and 29, Baji teaches a microcontroller wherein the incoming messages include multi-frame, fragmented messages, and the module automatically assembles the multi-frame, fragmented messages (figure 4 shows the multi-frame fragmented instructions handled by the DMAC).

11. As per claims 23 and 30, Baji teaches a microcontroller wherein the module

includes the memory-mapped registers (column 15, lines 16 – 19).

12. As per claims 24 and 31, Baji teaches a microcontroller wherein the processor core, the module, and the memory interface unit are contained on a single integrated circuit chip (figure 1).

13. As per claim 25, Baji teaches a microcontroller wherein the first and second memory segments are contained on the integrated circuit chip (figure 1).

14. As per claims 26 and 33, Baji teaches a microcontroller wherein the memory interface unit includes two independent arbiters (consists of more than two arbiters, figure 2).

15. As per claims 27, 34, 36 and 39 (interpreted with out the CAN/CAL environment) Baji teaches a microcontroller wherein the memory interface unit arbitrates access according to an alternate winner policy, wherein a previous loser is designated a current winner (initial access is granted based upon a priority scheme, and succeeding accesses are stalled and done in order of receipt, column 7, lines 1 – 34).

16. As per claim 32, Baji teaches a microcontroller wherein the second memory space provides at least a portion of the message buffer memory space (second memory

is included in the overall memory space by the DSP, column 5, lines 54 - 65).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 35 – 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baji in view of Upender et al (US Patent Number 5, 854, 454 hereinafter "Upender").

19. Claims 35 and 37 (interpreted with the CAN/CAL environment) Baji teaches a method for operating microcontroller with the same operation as in claim 28 above except having the type of microcontroller as CAN.

Baji does not disclose the microcontroller being of type CAN.

Upender teaches a CAN microcontroller following CAN protocols (column 1, CAN processor chips, lines 35 – 65).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify Baji with the above teachings of Upender. One would be motivated to make such modification in order to satisfy distributed real-time control needs (column 1, lines 35 – 43).

20. Baji modified by Upender as per claim 35 above, as per claims 38 and 40 (interpreted with out the CAN/CAL environment) Baji teaches a method for operating microcontroller with the same operation as in claim 28 above except having a module requesting access to be a CAN/CAL type module.

Baji does not disclose the module being of type CAN/CAL.

Upender teaches a CAN/CAL module requesting access (processing in accordance with CAN protocol messages, column 6, lines 5- 8)

21. Baji modified by Upender as per claim 35 above, as per claims 36 and 39, Baji teaches a microcontroller wherein the memory interface unit arbitrates access according to an alternate winner policy, wherein a previous loser is designated a current winner (initial access is granted based upon a priority scheme, and succeeding accesses are stalled and done in order of receipt, column 7, lines 1 – 34).

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 5,001,624 discloses processor controlled DMA transferring instruction and data from memory to processor. US Patent Number 5,099,417 discloses DMA and data processing. US Patent Number 5,179,689 discloses data processing with instruction cache. US Patent Number 6,041,387 discloses read/write access to registers having register-file access via CPU. US Patent Number

5,982,684 discloses parallel access to a memory array. XA User Guide discloses on and off-chip memory access with parallel instruction processing in a pipelined microcontroller. The aforementioned cited references all have elements of the current application.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KIM HUYNH
SUPERVISORY PATENT EXAMINER
8/21/06